

A New Modeling and Optimization of Gain-Boosted Cascode Amplifier for High-Speed and Low-Voltage Applications

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Abstract—Because of limited output swing, the basic structure of a gain-boosted cascode amplifier (GBCA) cannot be used to design a low-voltage operational amplifier. In this paper, we investigate the design of a high-swing GBCA, and find the optimum bandwidth for the boosting or feedback amplifier. This bandwidth eliminates the slow-settling component in the step response, prevents the gain-boosting loop from being unstable, and results in the shortest settling time. Finally, we present a very high-speed and high-swing amplifier suitable for low-voltage applications.

Index Terms—Analog circuits, cascode amplifier, CMOS, gain boosting.

I. INTRODUCTION

HIGH-performance, low-power amplifiers capable of operating at a supply voltage of 1.8 V or below are required as building blocks of portable mixed-signal systems. For fast and complete charge transfer, amplifiers in switched-capacitor circuits have to meet two requirements: high-speed and high open-loop gain. However, optimizing amplifiers for speed and gain leads to contradictory demands. The high-gain requirement leads to multistage designs with long-channel devices biased at low current levels, whereas the high-speed requirement calls for a single-stage design with short-channel devices biased at high current levels [1].

The gain-boosting technique [Fig. 1(a)] has enabled circuit designers to exploit the advantages of single-stage amplifiers with adequate gain. In the technique, the output resistance and the gain of the main cascode amplifier are increased considerably using a feedback amplifier (FA). However, if the FA is not properly designed, a low-frequency pole-zero frequency doublet will appear in the transfer function [1] of the main amplifier. Even though the doublet does not noticeably affect the frequency response, it introduces a very slow-settling component in the settling time, which is undesirable for many applications [2].

The proper design procedure of a gain-boosted cascode amplifier (GBCA) has been a subject of study during the past years [3]–[6]. All the methods and design rules presented thus far [3]–[6] are suitable for the basic GBCA structure shown in Fig. 1(b). However, the circuit has a limited output swing with low supply voltages. The limited output swing problem can be explained as follows: from Fig. 1(b), the lower end of the output

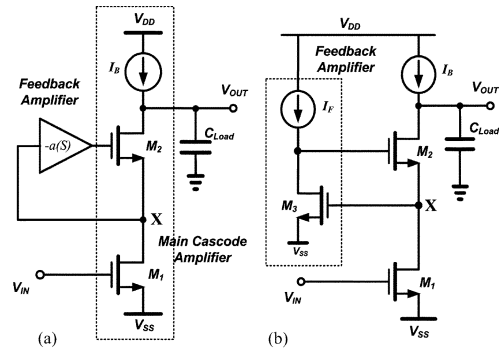


Fig. 1. (a) Enhancing the gain of a cascode stage using gain-boosting method. (b) Basic structure of a GBCA.

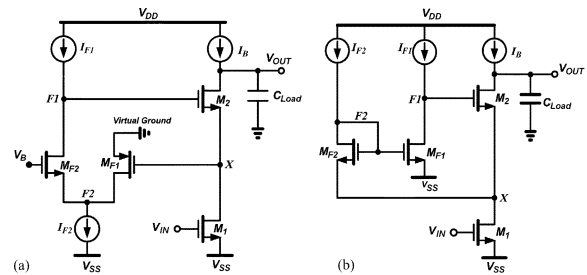


Fig. 2. High-swing GBCA using (a) a folded cascode FA, and (b) a voltage level shifter for FA.

swing is limited by $V_{GS3} + V_{DS2,sat}$, which is about 0.8 V in a typical 0.18- μm CMOS process. Since, the gain-boosting method, for being effective, should also be used for the current source I_B , a similar limitation exists for the upper end of the output swing. As a result, the allowable voltage swing at the output node is about 0.2 V with a 1.8-V supply voltage, which is not satisfactory for most applications. Hence, the previously proposed optimization methods are not useful in low-load circuit design.

There are some other GBCA structures for which the FA does not restrict the output swing (Fig. 2) [7], [8]. However, these structures suffer from a stability problem. In the structures shown in Fig. 2, the FA has at least two poles in its transfer function, i.e., a low-frequency pole at node $F1$ and a high-frequency pole at node $F2$. Since, in addition to those poles, there is another pole at node X, there are at least three poles in the gain-boosting loop consisted of the FA and transistor M_2 . This situation makes the gain-boosting loop very susceptible to instability.

In this paper, we study the optimum design criteria for designing a high-swing GBCA suitable for low-voltage applications. To the best of our knowledge, this is the first paper

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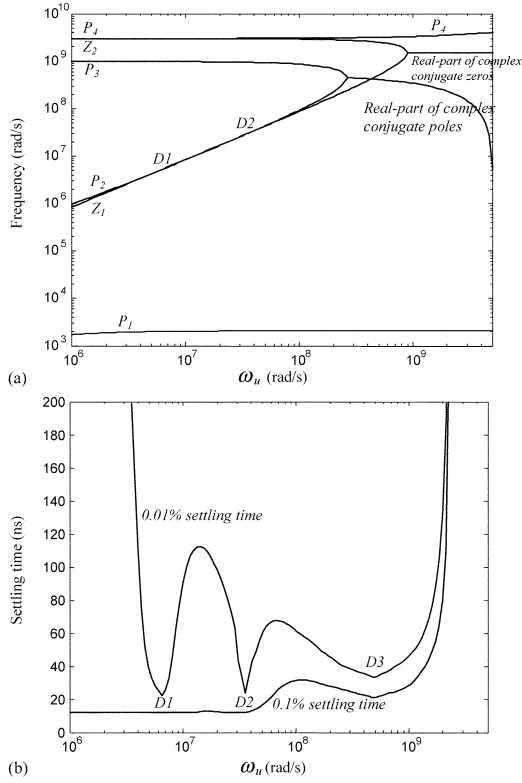


Fig. 4. (a) Pole-zero frequency locations, and (b) 0.1% and 0.01% settling times of an instance GBCA versus the GBW of the FA, ω_u ; for $a_0 = 200$, $C_L = 10$ pF, $C_X = 3$ pF, $g_{m1} = 4$ mS, $g_{m2} = 2.4$ mS, $g_{mb2} = 0.4$ mS, $g_{ds1} = 100$ μ S, $g_{ds2} = 50$ μ S, $G_L = 0.01$ μ S, and $P_{F2} = 3$ G rad/s.

(2). From the figure we can see that the doublet has no considerable effect on the settling time to 0.1% error band, but it degrades the settling to 0.01% error band drastically. This means that slow-settling component falls inside the 0.1% error band.

By increasing ω_u , at points $D1$ and $D2$ where pole and zero of the doublet cancel each other out, two minimum points occur in the 0.01% settling time. Although the doublet is very compressed between those points, it still considerably slows down the 0.01% settling time.

It may seem that the value of ω_u at points $D1$ and $D2$, i.e., ω_{D1} and ω_{D2} , are suitable bandwidths for the FA, however, at these points, the settling time is very sensitive to the value of ω_u . Besides, regarding (4), the value of ω_u at these points is proportional to the output conductance g_{ds} of transistors M_1 and M_2 . Since the output conductance g_{ds} of a transistor in a typical MOS technology is subject to large changes due to process variations, a designer is not able to exactly adjust ω_u equal to ω_{D1} and ω_{D2} .

Concluding, if we design a wide-band FA, the complex-conjugate pole pair is pushed to the RHP of complex plane and the gain-boosting loop will be unstable, on the other hand, if we design a low-bandwidth FA, the pole-zero doublet drastically slows down the precise settling times. In addition, designing a FA with a bandwidth equal to ω_{D1} or ω_{D2} does not solve the problem because of the dependency of ω_{D1} or ω_{D2} on the output conductance of transistors M_1 and M_2 . Thus, choosing a suitable bandwidth for the FA is very critical, especially in high-swing GBCA structures.

Fig. 4(b) clearly shows that by further increasing ω_u , another minimum point, $D3$, occurs in the 0.01% settling which, although is not as low as the other two minimum points, $D1$ and

$D2$, it is less sensitive to the value of ω_u . Hence, this point is the optimum value for ω_u . As we can see by comparing Fig. 4(a) and (b), at point $D3$, the doublet is replaced by a complex-conjugate pole pair.

Equation (2) is too complicated to be used for deriving the optimum criteria. As a result, we have to simplify it to be able to find the optimum bandwidth for the FA. Based on the observation we made in the previous section, we do following simplifications in $A(S)$ and mention their impacts.

- 1) The FA transfer function at high frequencies can be well approximated by [8]

$$a(S) \approx \frac{\omega_u}{S \left(1 + \frac{S}{P_{F2}}\right)}. \quad (5)$$

This simplification results in erroneous calculation of the dominant pole frequency of $A(S)$, P_1 , which is of no important consequence to the settling time.

- 2) The transconductance of a MOS transistor is much greater than its output conductance; i.e., $g_m \gg g_{ds}$. This simplification results in erroneous calculation of ω_{D1} and ω_{D2} , but this is also not important, because we already know that the optimum value of ω_u is not around ω_{D1} or ω_{D2} .

Considering the above simplifications in $A(S)$ and assuming a unity-gain feedback, the closed-loop transfer function of the GBCA, $H(S)$, is given by (6) shown at the bottom of the next page. By dividing the numerator and the denominator of (6) by $C_X C_L$ and recalling that $P_X = (g_{m2} + g_{mb2})/C_X$, and gain-bandwidth product of the whole amplifier is given by $\text{GBW} = g_{m1}/C_L$ [8], (6) can be rearranged to (7), shown at the bottom of the next page. If we normalize (7) to the GBW of the GBCA by the help of following equations:

$$\omega_{un} = \frac{\omega_u}{\text{GBW}}, \quad P_{Xn} = \frac{P_X}{\text{GBW}}, \quad P_{F2n} = \frac{P_{F2}}{\text{GBW}}, \quad S_n = \frac{S}{\text{GBW}} \quad (8)$$

we are able to convert (7) to a generic model for the GBCA given by (9) shown on the next page. Obtaining (9) enables us to easily consider the impacts of the important FA parameters, such as P_{F2} and ω_u , on the settling time of the GBCA

III. OPTIMUM DESIGN CRITERIA

In order to find the optimum design criteria for a GBCA, we should find an analytical expression for the settling time from the normalized closed-loop transfer function, $H_n(S)$. However, because of the potentially transcendental nature of the derived closed-loop transfer function, an analytical expression for the settling time can not be generally derived. The desperate approach is to sweep all parameters existing in $H_n(S)$ and find the best relation between those parameters giving the shortest settling time.

Three parameters, ω_{un} , P_{Xn} and P_{F2n} , are in $H_n(S)$. We have swept them in the practical range of interest and found the resulting settling time using MATLAB simulations. The P_{Xn} is the ratio of P_X , i.e., the second pole of the main cascode amplifier, over GBW, i.e., the gain-bandwidth product of the main amplifier. As a result, it can represent the phase margin (PM) of the main cascode amplifier. It can also represent the PM of the GBCA, because the FA has no significant effect on the frequency response [3]–[6]. The interest range for P_{Xn} is from 1.5 to 3.6, which corresponds to a PM of 60° to 75° .

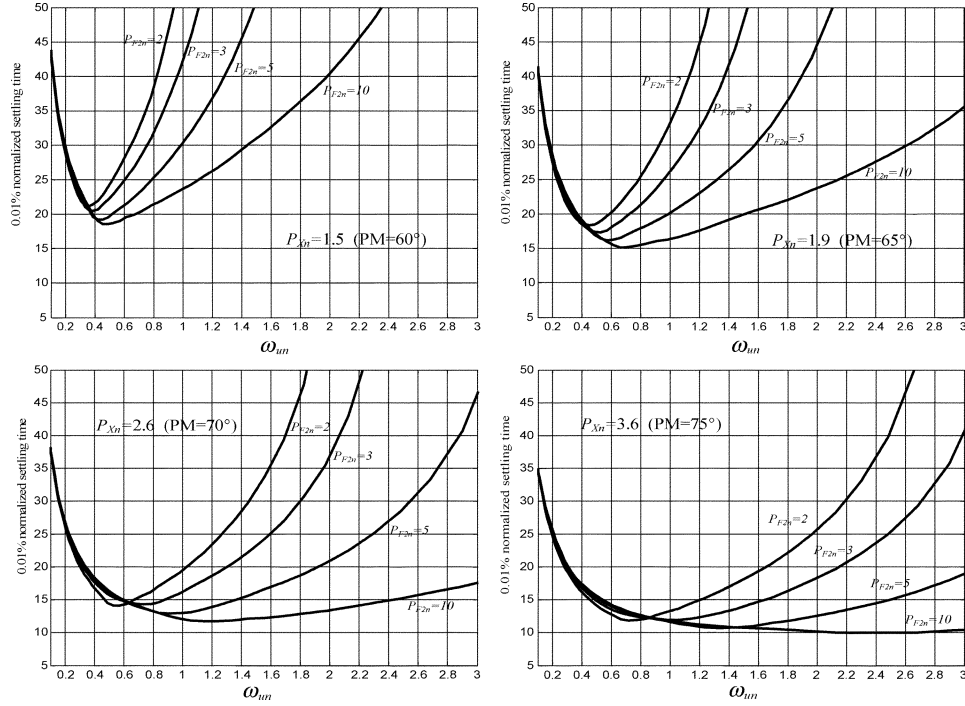


Fig. 5. 0.01% normalized settling time of the GBCA versus ω_{un} , for several values of P_{Xn} (PM of the main cascode amplifier), and P_{F2n} .

In addition, since the constraints for the design of the FA are fewer than those for the main cascode amplifier, P_{F2} can be potentially at very high frequencies compared to GBW and P_X ; as a result, we have swept P_{F2n} from 2 to 10.

By comparing the curves shown in Fig. 5, we can make the following observations: 1) pushing P_X and P_{F2} to higher frequencies reduces the minimum achievable settling time. Having $P_{Xn} < 2.6$ and $P_{F2n} < 5$ is not suitable for designing amplifiers with short 0.01% settling times. Besides, at a low P_{Xn} , the sensitivity of settling time to ω_{un} , at optimum ω_{un} , is relatively high. 2) If $P_{Xn} > 2.6$ and $P_{F2n} > 5$, then the FA bandwidth, ω_u , should be almost the same as that of the main cascode amplifier (sometimes a greater ω_u can have a better result, but increasing ω_u is power consuming; hence, we suffice to set $\omega_u = \text{GBW}$). 3) If $P_{Xn} > 2.6$ and $P_{F2n} > 5$, then the normalized settling time at optimum ω_u is almost between 10 and 12. Since all frequencies are normalized to GBW, settling times are normalized to GBW^{-1} .

As a result of above observations, a simple design procedure for designing a GBCA with a short 0.01% small-signal settling time equal to T_S seconds can be explained as follows: 1) design a simple cascode amplifier with a GBW [Hz] of $10/(2\pi T_S)$ and a phase margin higher than 70° ; 2) find the total capacitance seen at the gate of M_2 , i.e., $C_{GD2} + C_{GS2}$. This is the load capacitance of the FA; 3) design a FA with a bandwidth equal to (or even slightly greater than) the bandwidth of the main cascode amplifier (the exact optimum bandwidth for the FA should be determined from Fig. 5 based on the exact values of P_{Xn} and P_{F2n}); 3) push the second pole of the FA to a frequency greater than 5 times the GBW. That is, the PM of the FA should be more than 80° .

It should be noted that, in general, the load capacitance of the FA i.e., $C_{GD2} + C_{GS2}$ is much smaller than that of the main cascode amplifier, and since the bandwidths of the FA and the main cascode amplifier should be almost equal, in an optimum designed GBCA, the FA amplifier consumes much less power

$$\begin{aligned}
 H(S) &= \frac{A(S)}{1 + A(S)} \\
 &= (g_{m1}((g_{m2} + g_{mb2})S^2 + P_{F2}(g_{m2} + g_{mb2})S + g_{m2}\omega_u P_{F2})) / \\
 &\quad (C_L C_X S^4 + ((g_{m2} + g_{mb2})C_L + P_{F2}C_L C_X)S^3 + (g_{m2} + g_{mb2})(P_{F2}C_L + g_{m1})S^2 \\
 &\quad + ((g_{m2} + g_{mb2})P_{F2}g_{m1} + g_{m2}P_{F2}\omega_u C_L)S + g_{m1}g_{m2}\omega_u P_{F2})
 \end{aligned} \quad (6)$$

$$H(S) = \frac{P_X \text{GBW} \left(S^2 + P_{F2}S + P_{F2} \frac{\omega_u}{1+\eta} \right)}{S^4 + (P_X + P_{F2})S^3 + P_X(\text{GBW} + P_{F2})S^2 + P_X P_{F2} \left(\text{GBW} + \frac{\omega_u}{1+\eta} \right)S + P_X P_{F2} \text{GBW} \frac{\omega_u}{1+\eta}} \quad (7)$$

$$H_n(S) = \frac{P_{Xn} (S_n^2 + P_{F2n}S_n + P_{F2n}\omega_{un})}{S_n^4 + (P_{Xn} + P_{F2n})S_n^3 + P_{Xn}(1 + P_{F2n})S_n^2 + P_{Xn}P_{F2n}(1 + \omega_{un})S_n + P_{Xn}P_{F2n}\omega_{un}} \quad (9)$$

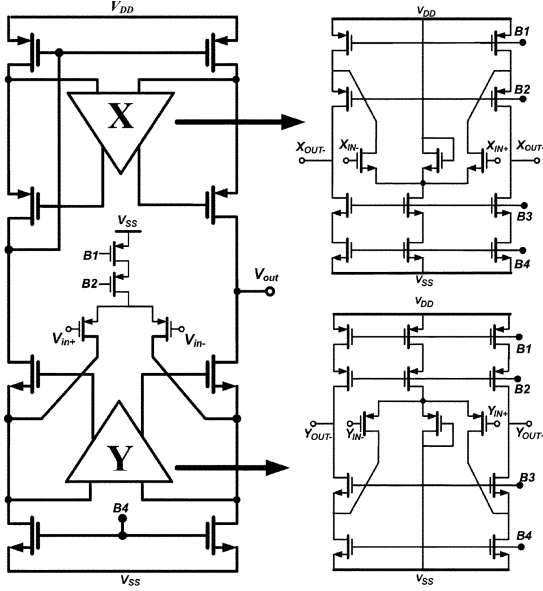


Fig. 6. Whole schematic of the designed high-speed low-voltage folded cascode amplifier (bias circuit is not depicted).

TABLE I
SUMMARY OF DESIGNED AMPLIFIER SPECIFICATIONS WITH $C_L = 1$ pF AND
1.8 V POWER SUPPLY VOLTAGE

Gain	80dB
GBW	660 MHz
Phase Margin	73°
0.1% Settling Time	1.7 nS
0.01% Settling Time	2.2 nS
Slew Rate	800 V/ μ S
Output Swing	1.2 V
Power dissipation	3.8 mW

compared with that of the main cascode amplifier. Due to the same reason, the g_m of the FA is much less than that of the main cascode amplifier; hence, the input transistor of the FA is very smaller than M_1 and it does not add a noticeable capacitance to node X. Thus, after adding FA to the main cascode amplifier, the P_X does not move noticeably.

IV. SIMULATION RESULTS

Based on the described design procedure, we have designed a very high-speed and low-power folded cascode operational amplifier in a 0.18- μ m CMOS process. The whole schematic of the amplifier is shown in Fig. 6. The amplifiers X and Y are feedback amplifiers which also have folded cascode structure. The actual length and width of the transistors are selected by the design procedure stated in [10]. Table I summarizes the specifications of the amplifier.

We have shown the step response of the amplifier in Fig. 7 when the FA bandwidth ω_u is optimum, is low, and is high. Fig. 7(a) clearly shows that when the bandwidths of the FAs are more than the optimum values, there is some ringing in the step response. If the bandwidths were increases more, the gain-boosting loops would be unstable. Fig. 7(b) shows the step response on an expanded scale to allow observation of 0.01% settling time. The figure obviously shows that when the bandwidths of FAs are low the slew-settling component introduced in step response causes a very slow settling to 0.01% error band.

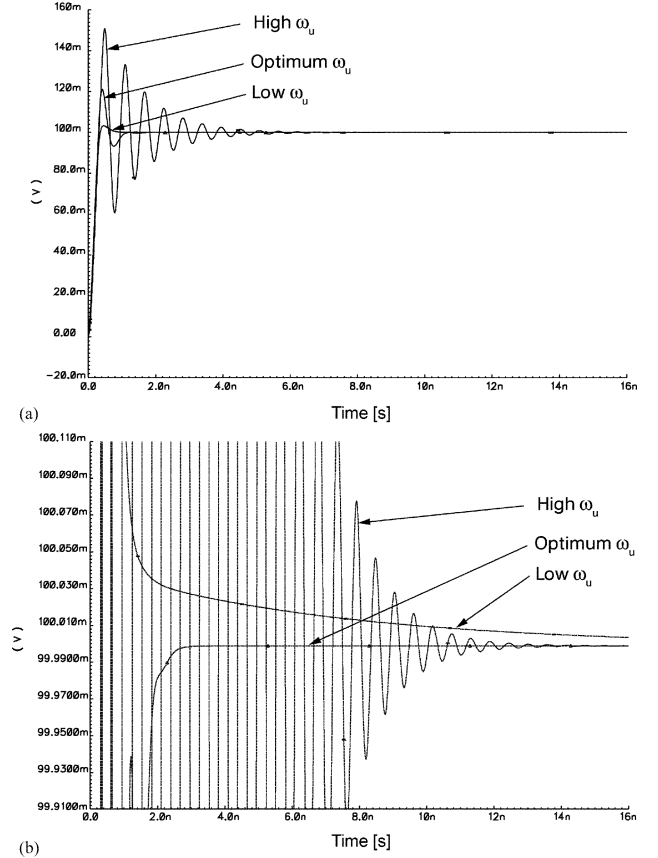


Fig. 7. (a) Step response of the designed amplifier with the optimum ω_u , a low ω_u , and a high ω_u . (b) The step response in an expanded scale.

V. CONCLUSION

In this paper, a novel and generic model for GB-CAs was developed. A method for optimum design of these amplifiers for high-speed applications was presented. This method is suitable for all types of gain-boosted cascode amplifiers, especially in low-voltage and low-power applications. Finally, a very high-speed and low-voltage amplifier was presented.

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